Rockchip RK3036S Datasheet

Revision 1.0
August 2024

Revision History

Date	Revision	Description
2024-08-19	1.0	Initial Release

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Chapter 1 Introduction

1.1 Overview

RK3036S is a low power, high performance processor solution for OTT TV BOX, and other digital multimedia applications, and integrates dual-core Cortex-A7, with separate NEON coprocessor and 128KB L2 Cache.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3036S supports almost full-format 1080P H.264 decoder and H.265 decoder, high-quality JPEG decoder and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3036S completely compatible with OpenGL ES1.1 and 2.0, OpenVG1.1 etc.

RK3036S has high-performance external memory interface (DDR3/DDR3L) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

1.2.1 Microprocessor

- Dual-core ARM Cortex-A7 MPCore processor, a high-performance, low-power and cached application processor.
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation.
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline.
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations.
- SCU ensures memory coherency between the two CPUs.
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- 128KByte unified L2 Cache.

1.2.2 Memory Organization

- Internal on-chip memory
  - 16KB BootRom
  - 8KB internal SRAM
- External off-chip memory①
  - DDR3-1066/DDR3L-1066, 16bits data width, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is 1GB.
  - Asynchronous Nand Flash(include LBA Nand), 8bits data width, 1 bank, 60bits ECC.

1.2.3 Internal Memory

- Internal BootRom
  - Size : 16KB
  - Support system boot from the following device:
    - 8bits Asynchronous Nand Flash
    - SPI Nand Flash
    - SPI Nor Flash
    - eMMC card
    - SD card
  - Support system code download by the following interface:
    - USB OTG interface
  - Support secure boot.

- Internal SRAM
  - Size : 8KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L)
  - Compatible with JEDEC standard DDR3/DDR3L SDRAM
  - Data rates up to1066Mbps(533MHz) for DDR3/DDR3L
  - Support up to 2 ranks (chip selects),maximum 1GB address space per rank
  - data width is 8bbits or 16bits, software programmable
  - Four host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/DDR3L SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3 /DDR3L SDRAM
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals, make SDRAM still in self-refresh state to prevent data missing

- Nand Flash Interface
  - Support asynchronous nand flash, each channel 8bits,1 bank
  - Support configurable interface timing
  - Embedded special DMA interface to do data transfer
  - Also support data transfer together with PERI_DMAC in SoC system

- eMMC Interface
  - Compatible with standard eMMC interface
  - Support MMC4.5 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support CRC generation and error detection
  - Embedded clock adjusting for high speed transfer
  - Support block size from 1 to 65535Bytes
  - Support 8bits data width with signal data rate or dual data rate

- SD/MMC Interface
  - Compatible with SD2.0, MMC4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock adjusting for high speed transfer
  - Support block size from 1 to 65535Bytes
  - Support 4bits data width signal data rate or dual data rate

- Serial Flash Controller(SFC)
  - One on-chip SFC inside RK3036S
  - Support command/address/data x1/x2/x4 bits mode configurable
  - Support 2 chip select
  - Support connected to serial nor flash or serial nand flash

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3036S
  - One oscillator with 24MHz clock input and three embedded PLLs: ARM PLL, DDR PLL, GENERAL PLL
  - Support global soft-reset control for whole SOC, also individual soft-reset for every

components

- Timer
  - Four on-chip 64bits Timers in SOC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - 24MHz or pclk_peri for clock input selectable

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - Five embedded AXI interconnect:
    - BUS interconnect
    - PERI interconnect
    - Display interconnect
    - GPU interconnect
    - VCODEC interconnect
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components inside RK3036S
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A7, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral,

peripheral-to-memory
- Signals the occurrence of various DMA events using the interrupt output signals
- Mapping relationship between each channel and different interrupt outputs is software-programmable
- One embedded DMA controller, PERI_DMAC is for peripheral system
- PERI_DMAC features:
  - 8 channels totally
  - 13 hardware request from peripherals
  - 2 interrupt output

1.2.6 Video CODEC

- Embedded memory management unit(MMU)
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, VP8, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 5.2 : 1080p@30fps (1920x1088)[3]
  - MPEG-4 up to ASP level 5 : 1080p@30fps (1920x1088)
  - MPEG-2 up to MP : 1080p@30fps (1920x1088)
  - MPEG-1 up to MP : 1080p@30fps (1920x1088)
  - H.263 : 576p@30fps (720x576)
  - VP8 : 1080p@30fps (1920x1088)
  - MVC : 1080p@30fps (1920x1088)
  - For H.264, image cropping not supported
  - For MPEG-4,GMC(global motion compensation)not supported
  - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.2.7 HEVC Decoder

- HEVC/H.265 decoder according to Main specification
- Support up to 1920x1088 (1080P@30fps) resolution
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.2.8 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[4] is up to 76million pixels per second
  - Embedded memory management unit(MMU)

1.2.9 Image Enhancement

- Image Post-Processor(embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory
  - Input data format:
    - Any format generated by video decoder in combined mode

- YCbCr4:2:0 semi-planar
- YCbCr4:2:0 planar
- YCbYCr 4:2:2
- YCrYCb 4:2:2
- CbYCrY 4:2:2
- CrYCbY 4:2:2

- Output data format:
  - YCbCr4:2:0 semi-planar
  - YCbYCr 4:2:2
  - YCrYCb 4:2:2
  - CbYCrY 4:2:2
  - CrYCbY 4:2:2
  - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888,RGB565,ARGB4444 etc.
- Input image size:
  - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
  - Stand-alone mode: width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
  - Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
- Support image up-scaling:
  - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Maximum output width is 3x input width
  - Maximum output height is 3x input height
- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (Allegro dither algorithm) for 4/5/6bit RGB channel precision
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

1.2.10 Graphics Engine

- 3D Graphics Engine(GPU)
  - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
  - Embedded 1 shader core with shared hierarchical tiler
  - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
  - Provide MMU and L2 Cache with 64KB size

1.2.11 Video OUT

- Display Interface
  - Display process
    - Background layer
      - programmable 24-bit color
    - Win0 (Video) layer
      - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
      - Support virtual display
      - 1/8 to 8 scaling-down and scaling-up engine

- ✧ Scale up using bicubic or bilinear
- ✧ Scale down using bilinear
- ✧ 1 Bicubic table: catrom
- ✧ coord 8bit, coe 8bit signed

- Win1 (UI) layer:
  - RGB888, ARGB888, RGB565
  - Support virtual display
- Hardware cursor:
  - 8bpp
  - Support two sizes: 32x32,64x64
- Overlay:
  - Win0/Win1 256 level alpha blending(support pre-multiplied alpha)
  - Win0/Win1 overlay position exchangeable
  - Win0/Win1 Transparency color key
  - Win0/Win1 global/per-pixel alpha
  - HWC 256 level alpha blending
  - HWC global/per-pixel alpha

- Others
  - Max output resolution: 1920x1080
  - Max scanning timing: 4096x4096
  - YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)and RGB2YcbCr
  - Support BCSH function
  - QoS request signals
  - Bus address alignment
  - Embedded memory management unit(MMU)

- HDMI TX
  - HDMI version 1.4a, HDCP revision 1.2 and DVI version 1.0 compliant transmitter
  - Supports DTV from 480i to 1080i/p HD resolution
  - Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
  - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
  - Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
  - S/PDIF output supports PCM and compressed audio transmission using IEC60958 and IEC61937
  - Multiphase 4MHz fixed bandwidth PLL with low jitter
  - HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
  - Support HDMI LipSync if needed
  - Lower power operation with optimal power management feature
  - The EDID and CEC function are also supported
  - Optional Monitor Detection supported through Hot Plug

- CVBS output
  - 10-bit Resolution
  - PAL/NTSC encoding
  - Programmable luma filter coefficient
  - Programmable luma/chroma delay
  - Programmable brightness/contrast

1.2.12 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX, 1xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable

- Support 3 I2S formats (normal, left-justified, right-justified)
- Support 4 PCM formats(early, late1, late2, late3)
- I2S and PCM mode cannot be used at the same time

- Audio CODEC
  - 24bit DAC with 95dB SNR
  - Support Line-out
  - Support Mono, Stereo, 5.1 HiFi channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1KHz/48KHz/96KHz
  - Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock

1.2.13 Connectivity

- SDIO interface
  - Embedded one SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus width

- SPI Controller
  - One on-chip SPI controller inside RK3036S
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- UART Controller
  - Three on-chip UART controllers inside RK3036S
  - DMA-based or interrupt-based operation
  - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation

- I2C controller
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - All of GPIOs can be used to generate interrupt to Cortex-A7
  - The pull direction(pullup or pulldown) for all of GPIOs are software-programmable
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength is not software-programmable, determined by the GPIO type; except special GPIOs for HDMI iomux

- USB Host2.0
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support up to 9 device mode endpoints in addition to control endpoint 0
  - Support up to 6 device mode IN endpoints including control endpoint 0
  - Endpoints 1/3/5/7 can be used only as data IN endpoint
  - Endpoints 2/4/6 can be used only as data OUT endpoint
  - Endpoints 8/9 can be used as data OUT and IN endpoint
  - Provides 9 host mode channels

1.2.14 Others

- eFuse
  - One 256bits high-density electrical Fuse, organized as 32x8bits
  - Program 1-bit each time in program mode
  - Read 8-bit each time in read mode
  - Three operation modes: program mode, read mode, inactive mode

- Package Type
  - BGA186(body: 9mm x 9mm; pin pitch: 0.65mm)

Notes:

① *DDR3/DDR3L are not used simultaneously*

② *In RK3036S, Video decoder and HEVC are not used simultaneously*

③ *Actual maximum frame rate will depend on the clock frequency and system bus performance*

④ *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3036S.

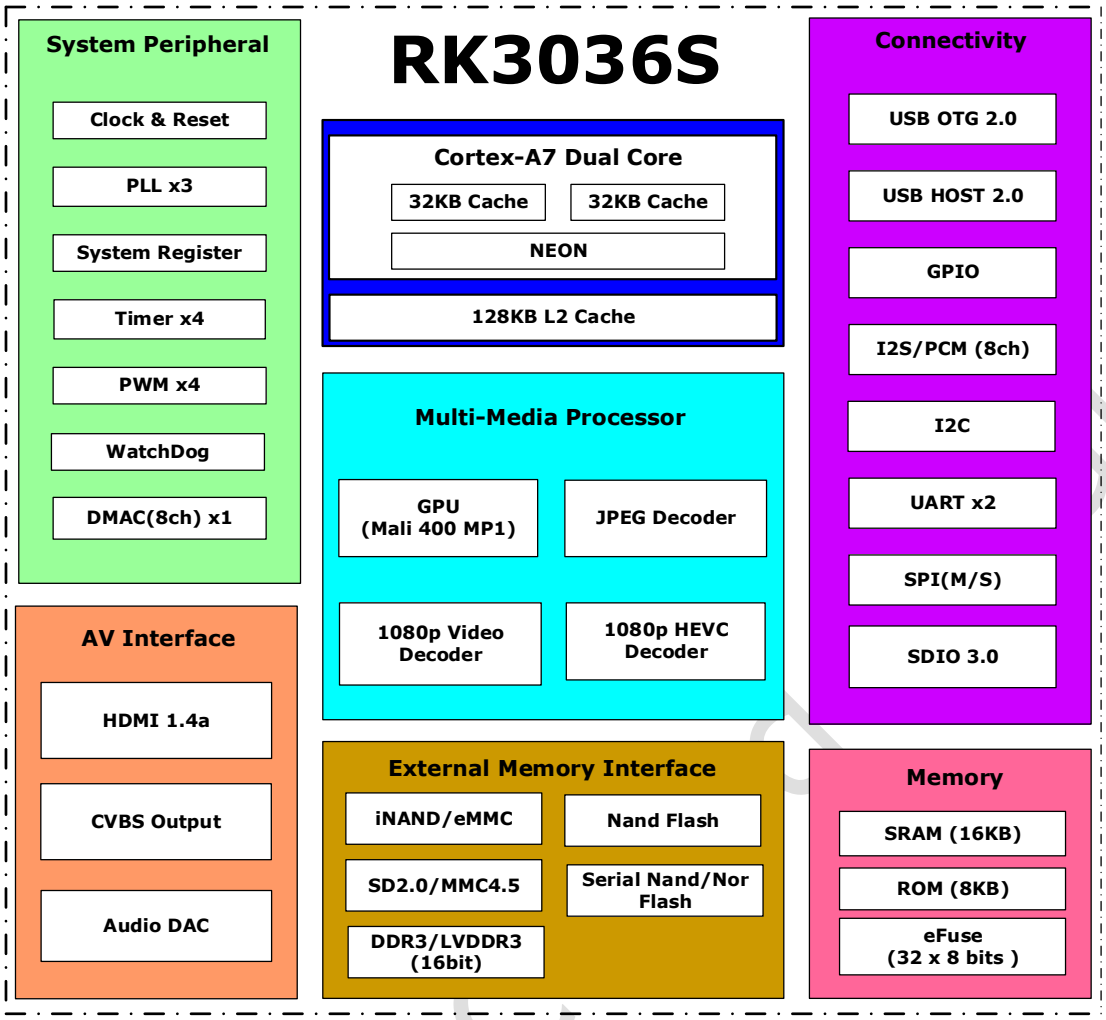


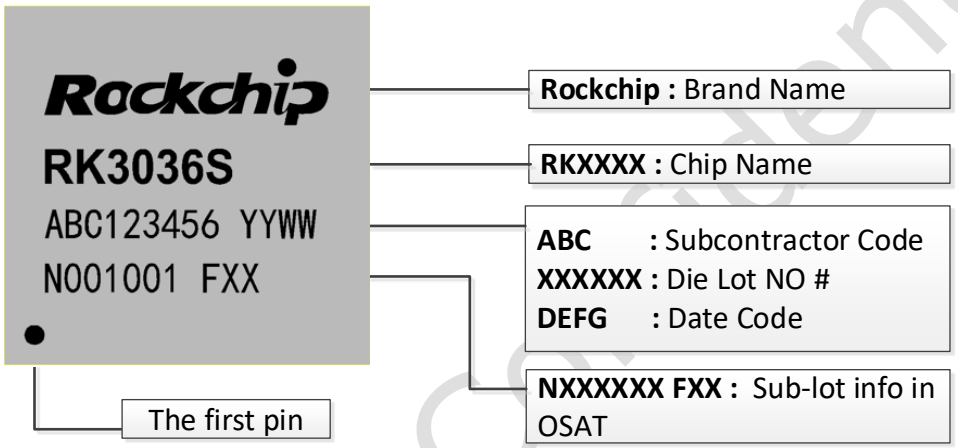
Fig. 1-1 RK3036S Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3036S	RoHS	TFBGA186	2600	Application processor

2.2 Top Marking



2.3 Dimension

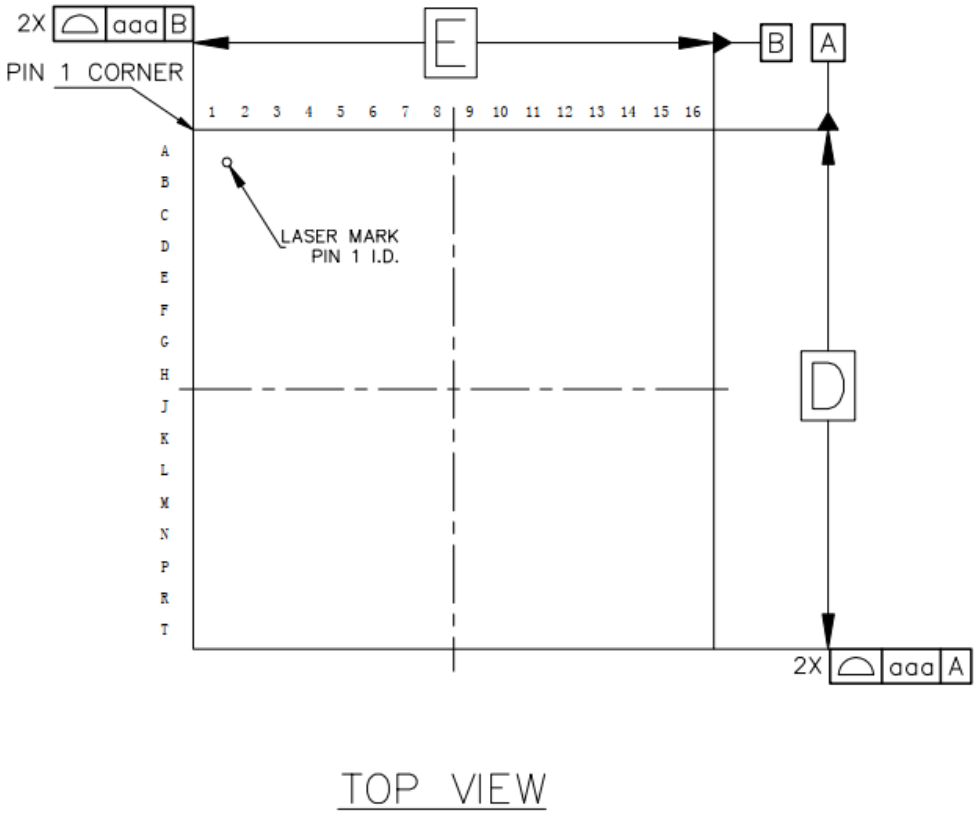
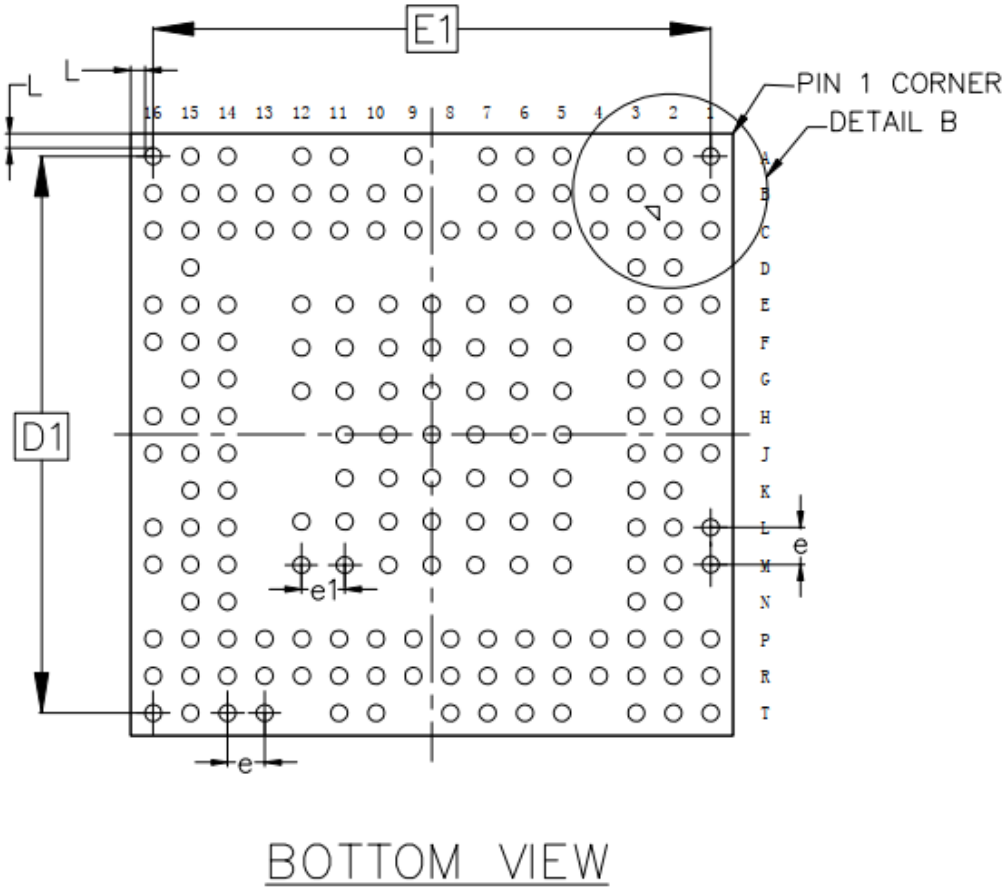


Fig. 2-1 RK3036S BGA186 Package Top View



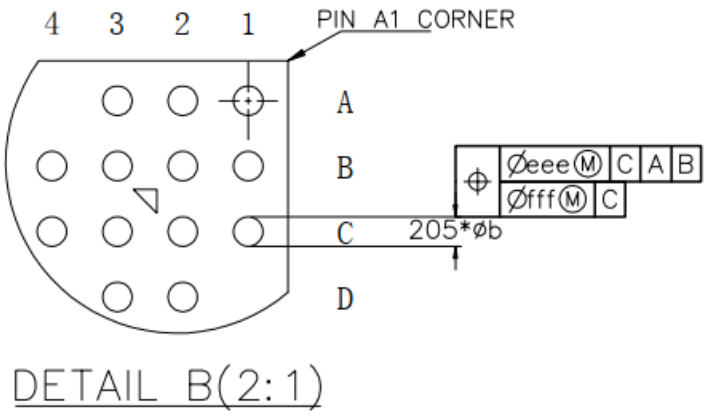


Fig. 2-2 RK3036S BGA186 Package Bottom View

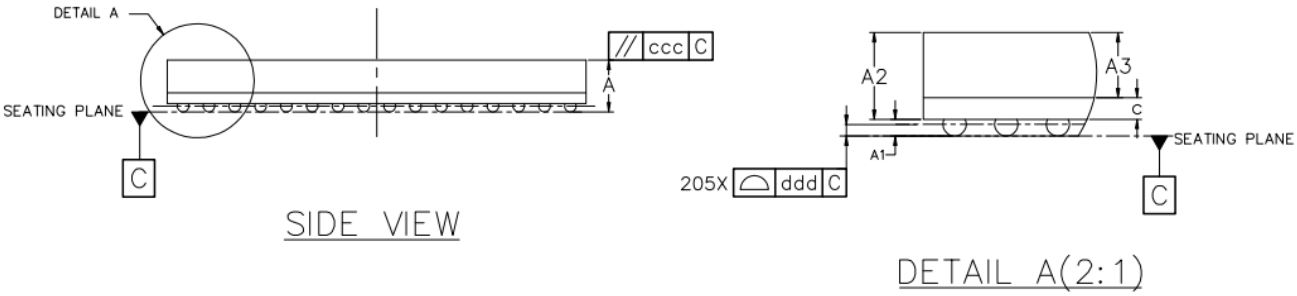


Fig. 2-3 RK3036S BGA186 Package Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.04	1.11	1.18
A1	0.13	0.18	0.23
A2	0.88	0.93	0.98
A3	0.70 BASIC		
c	0.20	0.23	0.26
D	8.90	9.00	9.10
D1	8.325 BASIC		
E	8.90	9.00	9.10
E1	8.325 BASIC		
e	0.555 BASIC		
e1	0.650 BASIC		
b	0.20	0.25	0.30
L	0.213 REF		
aaa	0.15		
ccc	0.08		
ddd	0.08		
eee	0.15		
fff	0.05		

Fig. 2-4 RK3036S BGA186 Package Dimension

2.4 MSL Information

Moisture sensitivity level：MSL3

2.5 Lead Finish/Ball Material Information

Lead finish/Ball material：SnAgCu

2.6 Pin List

Table 2-1 RK3036S BGA186 Pin List

Pin NO.	Pin Name	Pin NO.	Pin Name
1A1	DDR_VDD_0	E1	DDR_ODT0
1A2	DDR_VDD_1	E14	GPIO0_C3/UART0_CTSN_u
1A3	DDR_VDD_2	E15	GPIO0_C0/UART0_TX_d
1A4	DDR_VDD_3	E16	GPIO0_C1/UART0_RX_u
1A5	VSS_25	E2	VSS_9
1A6	CVDD_0	E3	DDR_BA2
1A7	CVDD_1	F14	GPIO0_B5/SDMMC1_D2/I2S1_SDI_u
1B1	DDR_CSN1	F15	GPIO0_C2/UART0_RTSN_u
1B2	VSS_26	F16	GPIO0_D3/IR_d
1B3	VSS_27	F2	VSS_10
1B4	VSS_28	F3	DDR_ODT1
1B5	VSS_29	G1	VSS_11
1B6	VSS_30	G14	GPIO0_B0/SDMMC1_CMD/I2S1_SDO_u
1B7	CVDD_2	G15	GPIO0_B6/SDMMC1_D3/I2S1_SCLK_u
1C1	CVDD_3	G2	DDR_DQ8
1C2	VSS_31	G3	DDR_DQ10
1C3	VSS_32	H1	DDR_DQS1_N
1C4	VSS_33	H14	VSS_12
1C5	VSS_34	H15	GPIO0_B1/SDMMC1_CLKO/I2S1_MCLK_u
1C6	VSS_35	H16	GPIO0_B3/SDMMC1_D0/I2S1_LRCK_RX_u
1C7	CVDD_4	H2	DDR_DQS1
1D1	PLL_VCCIO	H3	DDR_DM1

Pin NO.	Pin Name	Pin NO.	Pin Name
1D2	PLL_DVDD11	J1	DDR_DQ9
1D3	VSS_36	J14	GPIO1_C5/SDMMC0_D3/JTAG_TMS_u
1D4	VSS_37	J15	GPIO0_B4/SDMMC1_D1/I2S1_LRCK_TX_u
1D5	VSS_38	J16	GPIO1_C4/SDMMC0_D2/JTAG_TCK_u
1D6	VCCIO3	J2	DDR_DQ11
1E1	VCCIO1	J3	DDR_DQ14
1E2	EFUSE	K14	GPIO1_C0/SDMMC0_CLKO_d
1E3	VSS_39	K15	GPIO1_B7/SDMMC0_CMD_u
1E4	VSS_40	K2	DDR_DQ13
1E5	VSS_41	K3	VSS_13
1E6	VSS_42	L1	DDR_DQ12
1F1	USB_AVDD33	L14	GPIO1_C3/SDMMC0_D1/UART2_TX_u
1F2	TEST	L15	VSS_15
1F3	VSS_43	L16	GPIO1_C2/SDMMC0_D0/UART2_RX_u
1F4	VSS_44	L2	DDR_DQ15
1F5	VSS_45	L3	VSS_14
1F6	VCCIO2	M1	VSS_16
1F7	CVDD_5	M14	GPIO2_A0/FLASH_ALE/SPI_CLK_d
1G1	HDMI_AVDD33	M15	NPOR
1G2	CODEC_AVDD	M16	GPIO1_C1/SDMMC0_DET_u
1G3	VSS_46	M2	XOUT24M
1G4	VSS_47	M3	XIN24M
1G5	CVDD_6	N14	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0_u
1G6	CVDD_7	N15	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1_u
1G7	CVDD_8	N2	VSS_17
A1	VSS_0	N3	GPIO1_B0/HDMI_CEC_u
A11	DDR_A6	P1	GPIO1_B2/HDMI_SCL_u
A12	VSS_2	P10	VSS_20
A14	DDR_DQ1	P11	CODEC_AVSS
A15	DDR_DQ3	P12	GPIO0_A1/PWM2/I2C0_SDA_u

Pin NO.	Pin Name	Pin NO.	Pin Name
A16	VSS_3	P13	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2_u
A2	DDR_RESETN	P14	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD_u
A3	DDR_A0	P15	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0_u
A5	DDR_RASN	P16	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1_u
A6	DDR_CLK	P2	GPIO1_B3/HDMI_HPD_d
A7	VSS_1	P3	VSS_18
A9	DDR_A14	P4	USB_EXTR
B1	DDR_WEN	P5	HDMI_EXTR
B10	DDR_A8	P6	HDMI_DVDD1V1
B11	DDR_A4	P7	USB_DVDD11
B12	DDR_DQ5	P8	VSS_19
B13	DDR_DQ4	P9	CODEC_VCM
B14	DDR_DQ7	R1	GPIO1_B1/HDMI_SDA_u
B15	DDR_DQ6	R10	HDMI_TX2N
B16	DDR_DM0	R11	CODEC_AOL
B2	DDR_A7	R12	GPIO0_A0/PWM1/I2C0_SCL_u
B3	VSS_4	R13	GPIO2_A6/FLASH_CS0_u
B4	DDR_A13	R14	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK_u
B5	DDR_CASN	R15	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3_u
B6	DDR_CLK_N	R16	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD_u
B7	DDR_A10	R2	USB0_VBUS
B9	VSS_5	R3	USB1_DP
C1	DDR_A3	R4	USB0_DM
C10	DDR_A11	R5	USB0_DP
C11	DDR_BA1	R6	HDMI_TX3N
C12	VSS_7	R7	HDMI_TX0P
C13	DDR_DQ2	R8	HDMI_TX1N
C14	DDR_DQ0	R9	HDMI_TX1P
C15	DDR_DQS0	T1	VSS_21
C16	DDR_DQS0_N	T10	HDMI_TX2P

Pin NO.	Pin Name	Pin NO.	Pin Name
C2	DDR_A5	T11	CODEC_AOR
C3	DDR_A9	T13	GPIO2_A2/FLASH_WRN/SFC_CSN0_u
C4	DDR_A2	T14	GPIO2_A3/FLASH_RDN/SFC_CSN1_u
C5	VSS_6	T15	GPIO2_A1/FLASH_CLE/EMMC_CLK_d
C6	DDR_CKE	T16	VSS_24
C7	DDR_A15	T2	USB0_ID
C8	DDR_A1	T3	USB1_DM
C9	DDR_A12	T5	VSS_22
D15	VSS_8	T6	HDMI_TX3P
D2	DDR_BA0	T7	HDMI_TX0N
D3	DDR_CSN0	T8	VSS_23

2.7 Power/ground IO Description

Table 2-2 RK3036S Power/Ground IO Information

Group	Pin#	Description
GND	1A5, 1B2, 1B3, 1B4, 1B5, 1B6, 1C2, 1C3, 1C4, 1C5, 1C6, 1D3, 1D4, 1D5, 1E3, 1E4, 1E5, 1E6, 1F3, 1F4, 1F5, 1G3, 1G4, A1, A12, A16, A7, B3, B9, C12, C5, D15, E2, F2, G1, H14, K3, L15, L3, M1, N2, P10, P3, P8, T1, T16, T5, T8	Internal Core Ground, Digital IO Ground, Analog IO Ground
CVDD	1A6, 1A7, 1B7, 1C1, 1C7, 1F7, 1G5, 1G6, 1G7	Internal Core Power Digital GPIO Power
VCCIO	1D6, 1E1, 1F6	GPIO Power
DDR_VDD	1A1, 1A2, 1A3, 1A4	DDR3 Digital IO Power
PLL_DVDD11	1D2	DDR PLL Analog Power
PLL_VCCIO	1D1	PLL Power
USB_DVDD11	P7	USB OTG2.0/Host2.0 Digital Power
USB_AVDD33	1F1	USB OTG2.0/Host2.0 Analog Power
CODEC_AVDD	1G2	Audio Codec Analog Power
CODEC_AVSS	P11	Audio Codec Analog Ground
HDMI_AVDD33	1G1	HDMI Power
HDMI_DVDD1V1	P6	HDMI Power

2.8 Function IO Description

Table 2-3 RK3036S IO List

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
DDR_DQ0	A		DDR_DQ0	DRAM0 data port		
DDR_DQ1	A		DDR_DQ1	DRAM0 data port		
DDR_DQ2	A		DDR_DQ2	DRAM0 data port		
DDR_DQ3	A		DDR_DQ3	DRAM0 data port		
DDR_DQ4	A		DDR_DQ4	DRAM0 data port		
DDR_DQ5	A		DDR_DQ5	DRAM0 data port		
DDR_DQ6	A		DDR_DQ6	DRAM0 data port		
DDR_DQ7	A		DDR_DQ7	DRAM0 data port		
DDR_DQ8	A		DDR_DQ8	DRAM0 data port		
DDR_DQ9	A		DDR_DQ9	DRAM0 data port		
DDR_DQ10	A		DDR_DQ10	DRAM0 data port		
DDR_DQ11	A		DDR_DQ11	DRAM0 data port		
DDR_DQ12	A		DDR_DQ12	DRAM0 data port		
DDR_DQ13	A		DDR_DQ13	DRAM0 data port		
DDR_DQ14	A		DDR_DQ14	DRAM0 data port		
DDR_DQ15	A		DDR_DQ15	DRAM0 data port		
DDR_DQS0	A		DDR_DQS0	DRAM0 data strobe 0		
DDR_DQS0_N	A		DDR_DQS0_N	DRAM0 data strobe 0		
DDR_DQS1	A		DDR_DQS1	DRAM0 data strobe 1		
DDR_DQS1_N	A		DDR_DQS1_N	DRAM0 data strobe 1		
DDR_DM0	A		DDR_DM0	DRAM0 data mask 0		
DDR_DM1	A		DDR_DM1	DRAM0 data mask 1		
DDR_A0	A		DDR_A0	DRAM0 address port		
DDR_A1	A		DDR_A1	DRAM0 address port		
DDR_A2	A		DDR_A2	DRAM0 address port		
DDR_A3	A		DDR_A3	DRAM0 address port		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
DDR_A4	A		DDR_A4	DRAM0 address port		
DDR_A5	A		DDR_A5	DRAM0 address port		
DDR_A6	A		DDR_A6	DRAM0 address port		
DDR_A7	A		DDR_A7	DRAM0 address port		
DDR_A8	A		DDR_A8	DRAM0 address port		
DDR_A9	A		DDR_A9	DRAM0 address port		
DDR_A10	A		DDR_A10	DRAM0 address port		
DDR_A11	A		DDR_A11	DRAM0 address port		
DDR_A12	A		DDR_A12	DRAM0 address port		
DDR_A13	A		DDR_A13	DRAM0 address port		
DDR_A14	A		DDR_A14	DRAM0 address port		
DDR_A15	A		DDR_A15	DRAM0 address port		
DDR_CLK_N	A		DDR_CLK_N	DRAM0 differential clock output		
DDR_CLK	A		DDR_CLK	DRAM0 differential clock output		
DDR_BA0	A		DDR_BA0	DRAM0 bank select 0		
DDR_BA1	A		DDR_BA1	DRAM0 bank select 1		
DDR_BA2	A		DDR_BA2	DRAM0 bank select 2		
DDR_ODT0	A		DDR_ODT0	DRAM0 on die termination control 0		
DDR_ODT1	A		DDR_ODT1	DRAM0 on die termination control 1		
DDR_CSN0	A		DDR_CSN0	DRAM0 chip select 0		
DDR_CSN1	A		DDR_CSN1	DRAM0 chip select 1		
DDR_CKE	A		DDR_CKE	DRAM0 clock enable		
DDR_RASN	A		DDR_RASN	DRAM0 row address strobe output		
DDR_CASN	A		DDR_CASN	DRAM0 column address strobe output		
DDR_WEN	A		DDR_WEN	DRAM0 write enable strobe output		
DDR_RESETN	A		DDR_RESETN	DRAM0 reset output		
DDR_VDD1	AP		DDR_VDD1	DDR PHY power supply		
DDR_VDD2	AP		DDR_VDD2	DDR PHY power supply		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
DDR_VDD3	AP		DDR_VDD3	DDR PHY power supply		
DDR_VDD4	AP		DDR_VDD4	DDR PHY power supply		
DDR_VDD5	AP		DDR_VDD5	DDR PHY power supply		
DDR_VDD6	AP		DDR_VDD6	DDR PHY power supply		
NPOR	I	up	NPOR	System reset input		
TEST	I	down	TEST	Enter into test mode,default connect to VSS		
XOUT24M	O		XOUT24M	Oscillator 24MHz clock output		
XIN24M	I		XIN24M	Oscillator 24MHz clock input		
DPLL_DVDD11	AP		DPLL_DVDD11	DPLL analog power supply		
APLL_DVDD11	AP		APLL_DVDD11	APLL analog power supply		
PLL_VCCIO	AP		PLL_VCCIO	PLL power		
USB1_DP	A		USB1_DP	USB1 Data Plus port		
USB1_DM	A		USB1_DM	USB1 Data Minus port		
USB0_ID	A		USB0_ID	USB0 ID detect input,need external pull-up		
USB_EXTR	A		USB_EXTR	USB0 130 Ω Reference external resistance		
USB0_VBUS	A		USB0_VBUS	USB connected detect input		
USB0_DM	A		USB0_DM	USB0 Data Minus port		
USB0_DP	A		USB0_DP	USB0 Data Plus port		
USB_DVDD11	AP		USB_DVDD11	USB 1.1V analog core supply		
USB_AVDD33	AP		USB_AVDD33	USB 3.3V analog positive supply		
EFUSE	AP		EFUSE	EFUSE VQPS Power supply		
HDMI_TX3N	A		HDMI_TX3N	HDMI differential pixel clock negative		
HDMI_TX3P	A		HDMI_TX3P	HDMI differential pixel clock positive		
HDMI_TX0N	A		HDMI_TX0N	HDMI channel 0 differential serial data negative		
HDMI_TX0P	A		HDMI_TX0P	HDMI channel 0 differential serial data positive		
HDMI_TX1N	A		HDMI_TX1N	HDMI channel 1 differential serial data negative		
HDMI_TX1P	A		HDMI_TX1P	HDMI channel 1 differential serial data positive		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
HDMI_TX2N	A		HDMI_TX2N	HDMI channel 2 differential serial data negative		
HDMI_TX2P	A		HDMI_TX2P	HDMI channel 2 differential serial data positive		
HDMI_EXTR	A		HDMI_EXTR	HDMI reference current generate,connect a 2K %1 resistor to VSS.		
GPIO1_B0/HDMI_CEC	I/O	up	HDMI_CEC	HDMI CEC communication		
GPIO1_B3/HDMI_HPD	I/O	down	HDMI_HPD	HDMI Hot Plug Detection input		
GPIO1_B2/HDMI_SCL	I/O	up	HDMI_SCL	HDMI I2C serial port,need external pull-up		
GPIO1_B1/HDMI_SDA	I/O	up	HDMI_SDA	HDMI I2C serial port,need external pull-up		
HDMI_AVDD33	AP		HDMI_AVDD33	HDMI power supply		
HDMI_DVDD1V1_1	AP		HDMI_DVDD1V1_1	HDMI power supply		
HDMI_DVDD1V1_2	AP		HDMI_DVDD1V1_2	HDMI power supply		
CODEC_AOL	A		CODEC_AOL	Left channel output		
CODEC_AOR	A		CODEC_AOR	Right channel output		
CODEC_VCM	A		CODEC_VCM	CODEC VCM,connect 4.7uF capacitance to VSS		
CODEC_AVDD	AP		CODEC_AVDD	CODEC POWER		
CODEC_AVSS	AG		CODEC_AVSS	CODEC VSS		
GPIO0_A1/PWM2/I2C0_SDA	I/O	up	PWM2	CPU POWER dynamic voltage scaing control	I2C0_SDA	
GPIO0_A0/PWM1/I2C0_SCL	I/O	up	BT_HOST_WAKE	BT module wake up CPU	I2C0_SCL	
GPIO2_A7	I/O	down	MUTE_CTL	AUDIO out mute control		
GPIO2_B0	I/O	up	RECOVER	Low level into Recover		
GPIO2_B1	I/O	down	STANDBY_LED	STANDBY LED control		
GPIO2_B3	I/O	down				
GPIO0_D2	I/O	down	OTG_DRV	USB OTG power control output		
GPIO0_D3/IR	I/O	down	IR	IR receive input		
GPIO0_C4/DRIVE_VBUS	I/O	down	HOST_VBUS	USB HOST power control output		
GPIO0_C2/UART0_RTSN	I/O	up	UART0_RTSN	UART0 serial port, for BT module		
GPIO0_C3/UART0_CTSN	I/O	up	UART0_CTSN	UART0 serial port, for BT module		
GPIO0_C0/UART0_TX	I/O	down	UART0_TX	UART0 serial port, for BT module		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
GPIO0_C1/UART0_RX	I/O	up	UART0_RX	UART0 serial port, for BT module		
GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0	I/O	up	FLASH_D0	Nand Flash/EMMC data port	EMMC_D0	SFC_SIO0
GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1	I/O	up	FLASH_D1	Nand Flash/EMMC data port	EMMC_D1	SFC_SIO1
GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2	I/O	up	FLASH_D2	Nand Flash/EMMC data port	EMMC_D2	SFC_SIO2
GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3	I/O	up	FLASH_D3	Nand Flash/EMMC data port	EMMC_D3	SFC_SIO3
GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD	I/O	up	FLASH_D4	Nand Flash/EMMC data port	EMMC_D4	SPI_RXD
GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD	I/O	up	FLASH_D5	Nand Flash/EMMC data port	EMMC_D5	SPI_TXD
GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0	I/O	up	FLASH_D6	Nand Flash/EMMC data port	EMMC_D6	SPI_CSN0
GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1	I/O	up	FLASH_D7	Nand Flash/EMMC data port	EMMC_D7	SPI_CSN1
GPIO2_A0/FLASH_ALE/SPI_CLK	I/O	down	FLASH_ALE	Nand flash address latch enable		SPI_CLK
GPIO2_A1/FLASH_CLE/EMMC_CLK	I/O	down	FLASH_CLE	Nand flash command latch enable	EMMC_CLK	
GPIO2_A2/FLASH_WRN/SFC_CSN0	I/O	up	FLASH_WRN	Nand flash write enable		SFC_CSN0
GPIO2_A3/FLASH_RDN/SFC_CSN1	I/O	up	FLASH_RDN	Nand flash read enable		SFC_CSN1
GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK	I/O	up	FLASH_RDY	Nand flash read/busy output	EMMC_CMD	SFC_CLK
GPIO2_A6/FLASH_CS0	I/O	up	FLASH_CS0	Nand flash select0 port		
GPIO1_B7/SDMMC0_CMD	I/O	up	SDMMC0_CMD	SDMMC0 command output		
GPIO1_C0/SDMMC0_CLKO	I/O	down	SDMMC0_CLKO	SDMMC0 clock output		
GPIO1_C1/SDMMC0_DET	I/O	up	SDMMC0_DET	SDMMC0 detect input		
GPIO1_C2/SDMMC0_D0/UART2_RX	I/O	up	SDMMC0_D0	SDMMC0 data0 port	UART2_RX	
GPIO1_C3/SDMMC0_D1/UART2_TX	I/O	up	SDMMC0_D1	SDMMC0 data1 port	UART2_TX	
GPIO1_C4/SDMMC0_D2/JTAG_TCK	I/O	up	SDMMC0_D2	SDMMC0 data2 port	JTAG_TCK	
GPIO1_C5/SDMMC0_D3/JTAG_TMS	I/O	up	SDMMC0_D3	SDMMC0 data3 port	JTAG_TMS	
GPIO0_B0/SDMMC1_CMD/I2S1_SDO	I/O	up	SDMMC1_CMD	SDIO0 command output, for WIFI module	I2S1_SDO	
GPIO0_B1/SDMMC1_CLKO/I2S1_MCLK	I/O	up	SDMMC1_CLKO	SDIO0 clock output, for WIFI module	I2S1_MCLK	
GPIO0_B3/SDMMC1_D0/I2S1_LRCK_RX	I/O	up	SDMMC1_D0	SDIO0 data port, for WIFI module	I2S1_LRCK_RX	
GPIO0_B4/SDMMC1_D1/I2S1_LRCK_TX	I/O	up	SDMMC1_D1	SDIO0 data port, for WIFI module	I2S1_LRCK_TX	
GPIO0_B5/SDMMC1_D2/I2S1_SDI	I/O	up	SDMMC1_D2	SDIO0 data port, for WIFI module	I2S1_SDI	
GPIO0_B6/SDMMC1_D3/I2S1_SCLK	I/O	up	SDMMC1_D3	SDIO0 data port, for WIFI module	I2S1_SCLK	

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
VCCIO1	P		VCCIO1	CPU IO Power supply		
VCCIO2	P		VCCIO2	CPU IO Power supply		
VCCIO3	P		VCCIO3	CPU IO Power supply		
VCCIO4	P		VCCIO4	CPU IO Power supply		
CVDD1	P		CVDD1	CPU core power supply		
CVDD2	P		CVDD2	CPU core power supply		
CVDD3	P		CVDD3	CPU core power supply		
CVDD4	P		CVDD4	CPU core power supply		
CVDD5	P		CVDD5	CPU core power supply		
CVDD6	P		CVDD6	CPU core power supply		
CVDD7	P		CVDD7	CPU core power supply		
CVDD8	P		CVDD8	CPU core power supply		
CVDD9	P		CVDD9	CPU core power supply		
VSS1	G		VSS1	VSS		
VSS2	G		VSS2	VSS		
VSS3	G		VSS3	VSS		
VSS4	G		VSS4	VSS		
VSS5	G		VSS5	VSS		
VSS6	G		VSS6	VSS		
VSS7	G		VSS7	VSS		
VSS8	G		VSS8	VSS		
VSS9	G		VSS9	VSS		
VSS10	G		VSS10	VSS		
VSS11	G		VSS11	VSS		
VSS12	G		VSS12	VSS		
VSS13	G		VSS13	VSS		
VSS14	G		VSS14	VSS		
VSS15	G		VSS15	VSS		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
VSS16	G		VSS16	VSS		
VSS17	G		VSS17	VSS		
VSS18	G		VSS18	VSS		
VSS19	G		VSS19	VSS		
VSS20	G		VSS20	VSS		
VSS21	G		VSS21	VSS		
VSS22	G		VSS22	VSS		
VSS23	G		VSS23	VSS		
VSS24	G		VSS24	VSS		
VSS25	G		VSS25	VSS		
VSS26	G		VSS26	VSS		
VSS27	G		VSS27	VSS		
VSS28	G		VSS28	VSS		
VSS29	G		VSS29	VSS		
VSS30	G		VSS30	VSS		
VSS31	G		VSS31	VSS		
VSS32	G		VSS32	VSS		
VSS33	G		VSS33	VSS		
VSS34	G		VSS34	VSS		
VSS35	G		VSS35	VSS		
VSS36	G		VSS36	VSS		
VSS37	G		VSS37	VSS		
VSS38	G		VSS38	VSS		
VSS39	G		VSS39	VSS		
VSS40	G		VSS40	VSS		
VSS41	G		VSS41	VSS		
VSS42	G		VSS42	VSS		
VSS43	G		VSS43	VSS		

Pin Name	Pad type	IO Pull	Default function	Default function description	Function 2	Function 3
VSS44	G		VSS44	VSS		
VSS45	G		VSS45	VSS		
VSS46	G		VSS46	VSS		
VSS47	G		VSS47	VSS		
VSS48	G		VSS48	VSS		
VSS49	G		VSS49	VSS		
VSS50	G		VSS50	VSS		
VSS51	G		VSS51	VSS		
VSS52	G		VSS52	VSS		
VSS53	G		VSS53	VSS		
VSS54	G		VSS54	VSS		
VSS55	G		VSS55	VSS		
VSS56	G		VSS56	VSS		

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②:Output Drive Unit is mA, only Digital IO has drive value;

③:Reset state: I = input without any pull resistor,O = output without any pull resistor;

④: In RK3036S, all the IOs are in the same power supply;

⑤:NC: not connected;

⑥:Driver strength for these IOs is configurable; others are fixed and determined by IO type.

2.9 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK3036S IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset
SWJ-DP	jtag_tck	I	JTAG interface clock input/SWD interface clock input
	jtag_tms	I/O	JTAG interface TMS input/SWD interface data out
SD/MMC Host Controller	sdmmc0_clkout	O	sdmmc card clock
	sdmmc0_cmd	I/O	sdmmc card command output and response input
	sdmmc0_data*i* (*i*=0~3)	I/O	sdmmc card data input and output
	sdmmc0_detect_n	I	sdmmc card detect signal, 0 represents presence of card
SDIO Host Controller	sdio_clkout	O	sdio card clock
	sdio_cmd	I/O	sdio card command output and response input
	sdio_data*i* (*i*=0~3)	I/O	sdio card data input and output
eMMC Interface	emmc_clkout	O	emmc card clock
	emmc_cmd	I/O	emmc card command output and response input
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output
DMC	DDR_CK	O	Active-high clock signal to the memory device
	DDR_CK_N	O	Active-low clock signal to the memory device
	DDR_CKE*i*	O	Active-high clock enable signal to the memory device for two chip select
	DDR_CSN*i* (*i*=0,1)	O	Active-low chip select signal to the memory device. There are two chip select
	DDR_RASN	O	Active-low row address strobe to the memory device
	DDR_CASN	O	Active-low column address strobe to the memory device
	DDR_WEN	O	Active-low write enable strobe to the memory device
	DDR_BA[2:0]	O	Bank address signal to the memory device
	DDR_ADDR[15:0]	O	Address signal to the memory device
	DDR_DQ[15:0]	I/O	Bidirectional data line to the memory device.
	DDR_DQS[3:0]	I/O	Active-high bidirectional data strobes to the memory device
	DDR_DQS_B[3:0]	I/O	Active-low bidirectional data strobes to the memory device
	DDR_DM[3:0]	O	Active-low data mask signal to the memory device
	DDR_ODT*i* (*i*=0,1)	O	On-Die Termination output signal for two chip select
	DDR_RESET	O	DDR3 reset signal to the memory device
NandC	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal

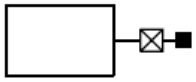
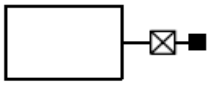
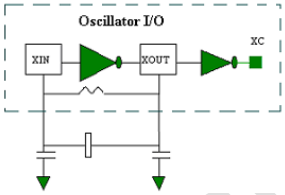
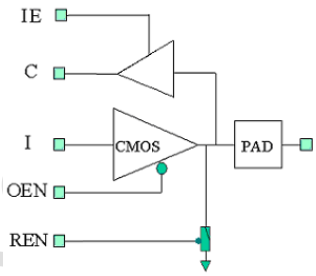
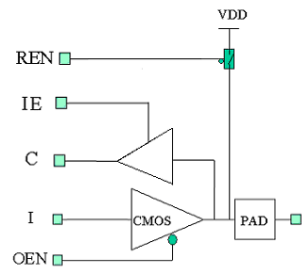
Interface	Pin Name	Direction	Description
	flash_data*i*(*i*=0~7)	I/O	Flash data inputs/outputs signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn0	O	Flash chip enable signal for chip0
SFC	sfc_clk	O	Serial flash clock
	sfc_csn*i*(*i*=0,1)	O	Serial flash chip enable signal for chip *i*(*i*=0,1)
	sfc_sio*i*(*i*=0~3)	I/O	Serial flash data inputs/outputs signal
I2S/PCM Controller	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrckrx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_lrcktx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo*i*(*i*=0~3)	O	I2S/PCM serial data output
SPI Controller	spi_clk	I/O	SPI serial clock
	spi_csn*i*(*i*=0,1)	I/O	SPI chip select signal,low active
	spi_txd	O	SPI serial data output
	spi_rxd	I	SPI serial data input
PWM	pwm3	O	Pulse Width Modulation output
	pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
UART	uart0_sin	I	UART0serial data input
	uart0_sout	O	UART0serial data output
	uart0_ctsn	I	UART0 clear to send
	uart0_rtsn	O	UART0 request to send
	uart2_sin	I	UART2serial data input
	uart2_sout	O	UART2serial data output
USB OTG 2.0	USB0PP	I/O	USB OTG 2.0 Data signal DP
	USB0PN	I/O	USB OTG 2.0 Data signal DM
	USB0ID	I	USB OTG 2.0 ID indicator
	VBUS_0	N/A	USB OTG 2.0 5V power supply pin
USB Host 2.0	USB1PP	I/O	USB HOST 2.0 Data signal DP
	USB1PN	I/O	USB HOST 2.0 Data signal DM
	VBUS_1	N/A	USB HOST 2.0 5V power supply pin
	USB_EXTR	N/A	130R Ohm Reference external resistance
eFuse	EFUSE_AVDD	N/A	eFuse program and sense power
HDMI	EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	TX0N	O	TMDS channel 0 negative data line
	TX0P	O	TMDS channel 0 positive data line
	TX1N	O	TMDS channel 1 negative data line

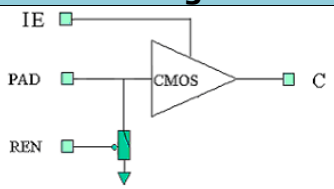
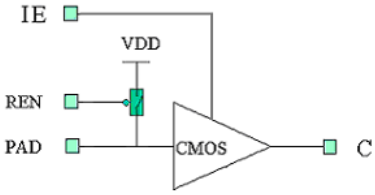
Interface	Pin Name	Direction	Description
	TX1P	O	TMDS channel 1 positive data line
	TX2N	O	TMDS channel 2 negative data line
	TX2P	O	TMDS channel 2 positive data line
	TX3N	O	TMDS negative clock line
	TX3P	O	TMDS positive clock line
Audio CODEC	VCM	I	Reference voltage input
	VOUTL	O	Left channel headphone output
	VOUTR	O	Right channel headphone output
Video DAC	IREF	I/O	Reference current. Output current when using External Reference Resistor or Input Reference Current when using external current source
	IOUTP0	O	Positive output
	IOUTN0	O	Negative output

2.10 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 RK3036S IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRN)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRN)

Type	Diagram	Description	Pin Name
F		controllable input pad with controllable pulldown	Part of digital GPIO (PICDRN)
G		controllable input pad with controllable pullup	Part of digital GPIO (PICURN)

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK3036S absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	CVDD, HDMI_DVDD1V1_1, HDMI_DVDD1V1_2, HDMI_DVDD1V1_3, HDMI_DVDD1V1_4 USB_DVDD11	1.4	V
DC supply voltage for Digital GPIO (except for PLL, USB, DDR, ACODEC, HDMI IO)	VCCIO	3.63	V
DC supply voltage for DDR IO	DDR_VDD	1.575	V
DC supply voltage for Analog part of PLL	PLL_VCCIO	3.63	V
DC supply voltage for Analog part of PLL	APLL_DVDD11,DPLL_DVDD11	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD33	3.63	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5.25	V
Digital input voltage for input buffer of GPIO		3.63	V
Digital output voltage for output buffer of GPIO		3.63	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

The following table describes the recommended operating conditions.

Table 3-2 RK3036S recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	CVDD, HDMI_DVDD1V1_1, HDMI_DVDD1V1_2, HDMI_DVDD1V1_3, HDMI_DVDD1V1_4 USB_DVDD11	0.99	1.1	TBD	V
Digital GPIO Power(3.3V)	VCCIO	2.97	3.3	3.63	V
DDR IO (DDRIII mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (LVDDRIII mode) Power	DDR_VDD	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	APLL_DVDD11,DPLL_DVDD11	0.99	1.1	1.21	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	117	130	143	Ohm
Acodec Analog Power	CODEC_AVDD	2.97	3.3	3.63	V
HDMI Analog Power	HDMI_AVDD33	2.97	3.3	3.63	V
EFUSE programming voltage		N/A	2.5	N/A	V
PLL input clock frequency		N/A	24	N/A	MHz
Max frequency of CPU				1.0	GHz
Max frequency of GPU				400	MHz
Ambient Operating Temperature	Ta	0	25	80	℃

Notes：① Symbol name is same as the pin name in the io descriptions

② With the reference software setup, the reference software will limit the chipset temperature about 80℃

3.3 DC Characteristics

Table 3-3 RK3036S DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	V_{IL}	-0.3		0.8	V
	Input High Voltage	V_{IH}	2		VDD+0.3	V
	Output Low Voltage	V_{OL}			0.4	V
	Output High Voltage	V_{OH}	2.4			V
	Pullup Resistor	R_{PU}	27	41	64	Kohm
	Pulldown Resistor	R_{PD}	31	46	78	Kohm
DDR IO @DDR3 mode	Input High Voltage	V_{ih_ddr}	VREFi + 0.125 (i=0~2)	1.5	VDDIO_DDRi + 0.3 (i=0~6)	V
	Input Low Voltage	V_{il_ddr}	-0.3	0	VREFi - 0.125 (i=0~2)	V
	Output High Voltage	V_{oh_ddr}	VDDIO_DDRi - 0.28 (i=0~6)	1.5	N/A	V
	Output Low Voltage	V_{ol_ddr}	N/A	0	0.28	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	120 60 40	150 75 50	180 90 60	Ohm
HDMI	Single-ended high level output voltage, (when sink <=165Mhz)	V_H	HDMI_AVDD 33-10mv		HDMI_AVDD 33+10mv	mv
	Single-ended high level output voltage, (when sink >165Mhz)	V_H	HDMI_AVDD 33-200mv		HDMI_AVDD 33+10mv	mv
	Single-ended low level output voltage, (when sink <=165Mhz)	V_L	HDMI_AVDD 33-600mv		HDMI_AVDD 33-400mv	mv
	Single-ended low level output voltage, (when sink >165Mhz)	V_L	HDMI_AVDD 33-700mv		HDMI_AVDD 33-400mv	mv
	Single-ended output swing voltage	$V_{s\ wing}$	400		600	mv
	Single-ended standby (off) output voltage	V_{OFF}		HDMI_AVDD 33+10mv		mv
	Single-ended standby (off) output current	I_{OFF}	-10		10	uA
PLL	Input High Voltage	V_{ih_pll}	0.8*DVDD_iPLL (i=A,D,G)	DVDD_iPLL (i=A,D,G)	DVDD_iPLL (i=A,D,G)	V
	Input Low Voltage	V_{il_pll}	0	0	0.2*DVDD_iPLL (i=A,D,G)	V

3.4 Recommended Operating Frequency

Table 3-4 Recommended operating frequency for PD_BUS domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
DDR PLL	1.0V , 25 ℃	ddr_pll_clk			1600	MHz
	1.1V , -40 ℃					
	0.9V , 125 ℃		800			
ARM PLL	1.0V , 25 ℃	arm_pll_clk			1600	MHz
	1.1V , -40 ℃					
	0.9V , 125 ℃		900			
GENERAL PLL	1.0V , 25 ℃	general_pll_clk			1400	MHz
	1.1V , -40 ℃					
	0.9V , 125 ℃		600			

3.5 Electrical Characteristics for General IO

Table 3-5 RK3036S Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	I_L	Vin = 3.3V or 0V			±10	uA
	Tri-state output leakage current	I_{OZ}	Vout = 3.3V or 0V			±10	uA
	High level input current	L_{IH}	Vin = 3.3V, pulldown disabled				mA
			Vin = 3.3V, pulldown enabled				mA
	Low level input current	L_{IL}	Vin = 0V, pullup disabled				mA
			Vin = 0V, pullup enabled				mA

3.6 Electrical Characteristics for PLL

Table 3-6 RK3036S Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @3.3V/1.1V	10		800	MHz
	Comparison frequency	F_{ref}	FREF = Fin/REFDIV @3.3V/1.1V	1		40	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	400		1600	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	1		1600	MHz
	Lock time	T_{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		1000	1500	Inputclockcycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V, 25 ℃ Current scale as $(Fvco/1GHz)^{1.5}$		0.8	1.0	mA
	VDD Power consumption (normal mode)		@3.3V/1.1V, 25 ℃		3	4	uW/MHz
	Power consumption (bypass mode)		BYPASS=HIGH , PD= LOW , Fin = 24MHz, Fout = 24MHz, @3.3V/1.1V, 25 ℃				uW
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		10		uA

Notes :

①:REFDIV is the input divider value;

FBDIV is the feedback divider value;
POSTDIV is the output divider value

3.7 Electrical Characteristics for USB Interface

Table 3-7 RK3036S Electrical Characteristics for USB Interface

Parameters		Symbol	Test condition	Min 2xport	Typ 2xport	Max 2xport	Units
USB	Supply current, low speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	24	26	29	mA
			TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	45	48	50	mA
			RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	40	43	46	mA

Parameters		Symbol	Test condition	Min 2xport	Typ 2xport	Max 2xport	Units
	Supply current, full speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	25	28	30	mA
			TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	55	59	63	mA
			RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	50	52	54	mA
	Supply current, high speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	33	35	38	mA
			TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	65	69	73	mA
			RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	50	54	56	mA
	Supply current, suspend		USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V		20	32	uA

3.8 Electrical Characteristics for DDR IO

Table 3-8 RK3036S Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	VDDIO_DDR standby current, ODT OFF		@ 1.5V , 125℃				uA
	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃				uA
DDR IO @LVDDR3 mode	Input leakage current		@ 1.35V,125℃				uA
	VDDquiescent current		@ 1.35V,125℃				uA

3.9 Electrical Characteristics for eFuse

Table 3-9 RK3036S Electrical Characteristics for eFuse

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Standby current	$I_{standby}$		-	1	-	uA
Peak burning current	I_{prog}		-	15	-	mA
Current duringnormal reading	I_{active}	10MHz	-	4	-	mA

3.10 Electrical Characteristics for HDMI

Table 3-10 RK3036S Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Rise time/fall time (20%-80%)			75		0.4*T_{bit}	ps
Overshoot, max			15% of full differential amplitude (Vswing *2)			mv
Undershoot, max			20% of full differential amplitude (Vswing *2)			mv
Intra-Pair Skew at Transmitter Connector, max			0.15 * T_{bit}			ps
Inter-Pair Skew at Transmitter Connector, max			0.20 * T_{bit}			ps
TMDS Differential Clock Jitter, max			0.25 * T_{bit}			ps
Clock duty cycle			40%		60%	

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3036S has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RK3036S. The resulting simulation data for reference only, please prevail in kindtest.

Table 4-1 RK3036S Thermal Resistance Characteristics

Package (TFBGA186)	$\theta_{JA}(℃/W)$	$\theta_{JB}(℃/W)$	$\theta_{JC}(℃/W)$
RK3036S	37	25.7	6.8

Note: The testing PCB is based on 4 layers, 114.3mmx 101.6mm, 1.6 mm Thickness, Ambient temperature is 40 ℃.

